

FIG. 2

FIG. 3 is a block diagram of a system 300, according to one embodiment. The system 300 includes a processor subsystem 320, a configuration switch 306, a storage device 324, a CPU 322, NVRAM 326, a processor bus 318, an I2C bus 328, a processor interface 312, an init agent 310, a system management agent (SMA) 308, a decoder 304, a system management processor (SMP) 332, and an agent 346. The processor subsystem 320 is connected to the processor bus 318 and the I2C bus 328. The configuration switch 306 is connected to the processor bus 318. The storage device 324 and CPU 322 are connected to the processor bus 318. The NVRAM 326 is connected to the I2C bus 328. The processor interface 312 is connected to the processor bus 318 and the I2C bus 328. The init agent 310 is connected to the processor interface 312. The SMA 308 is connected to the init agent 310. The decoder 304 is connected to the processor bus 318 and the I2C bus 328. The SMP 332 is connected to the decoder 304. The agent 346 is connected to the I2C bus 328.

300

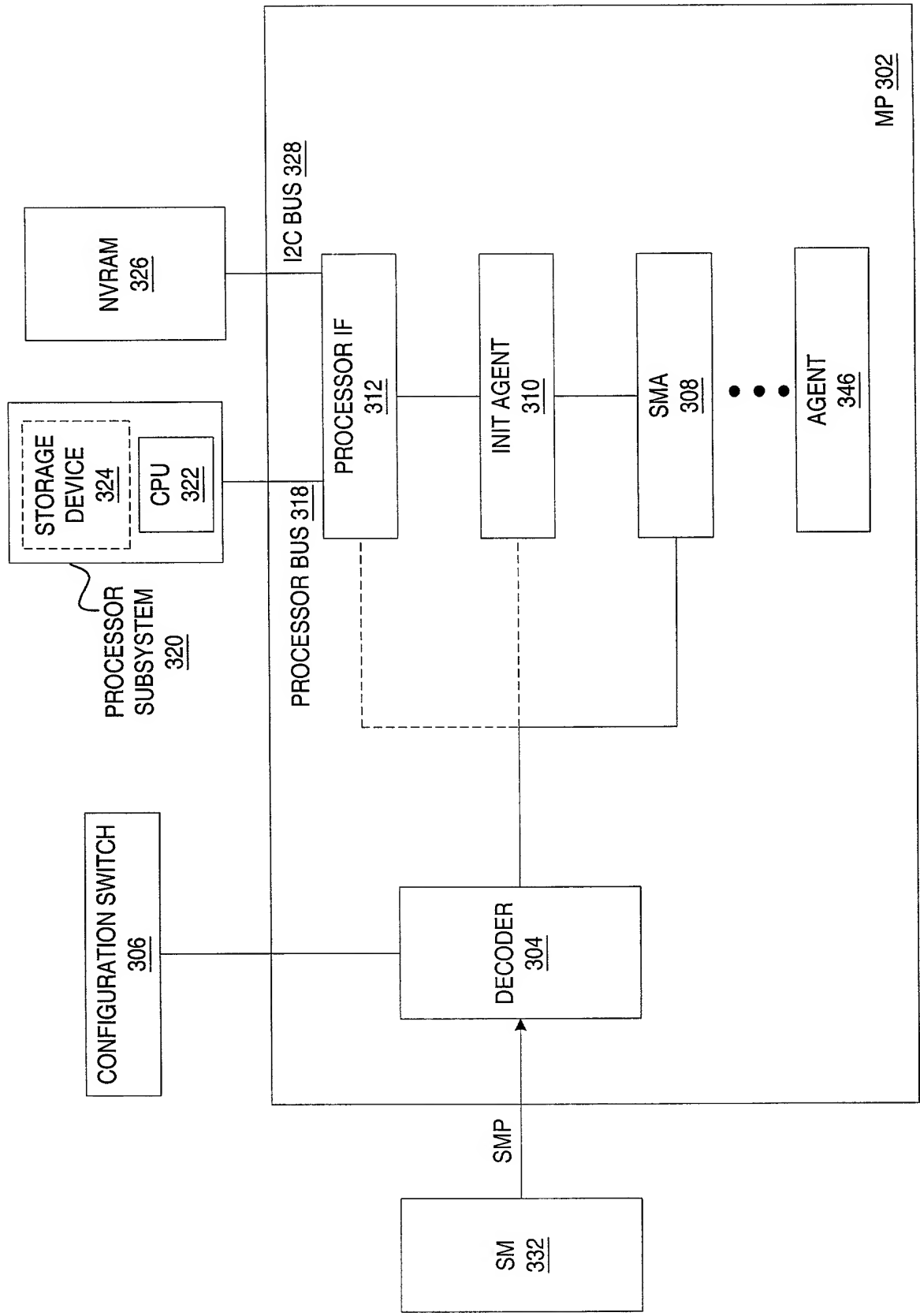


FIG. 3

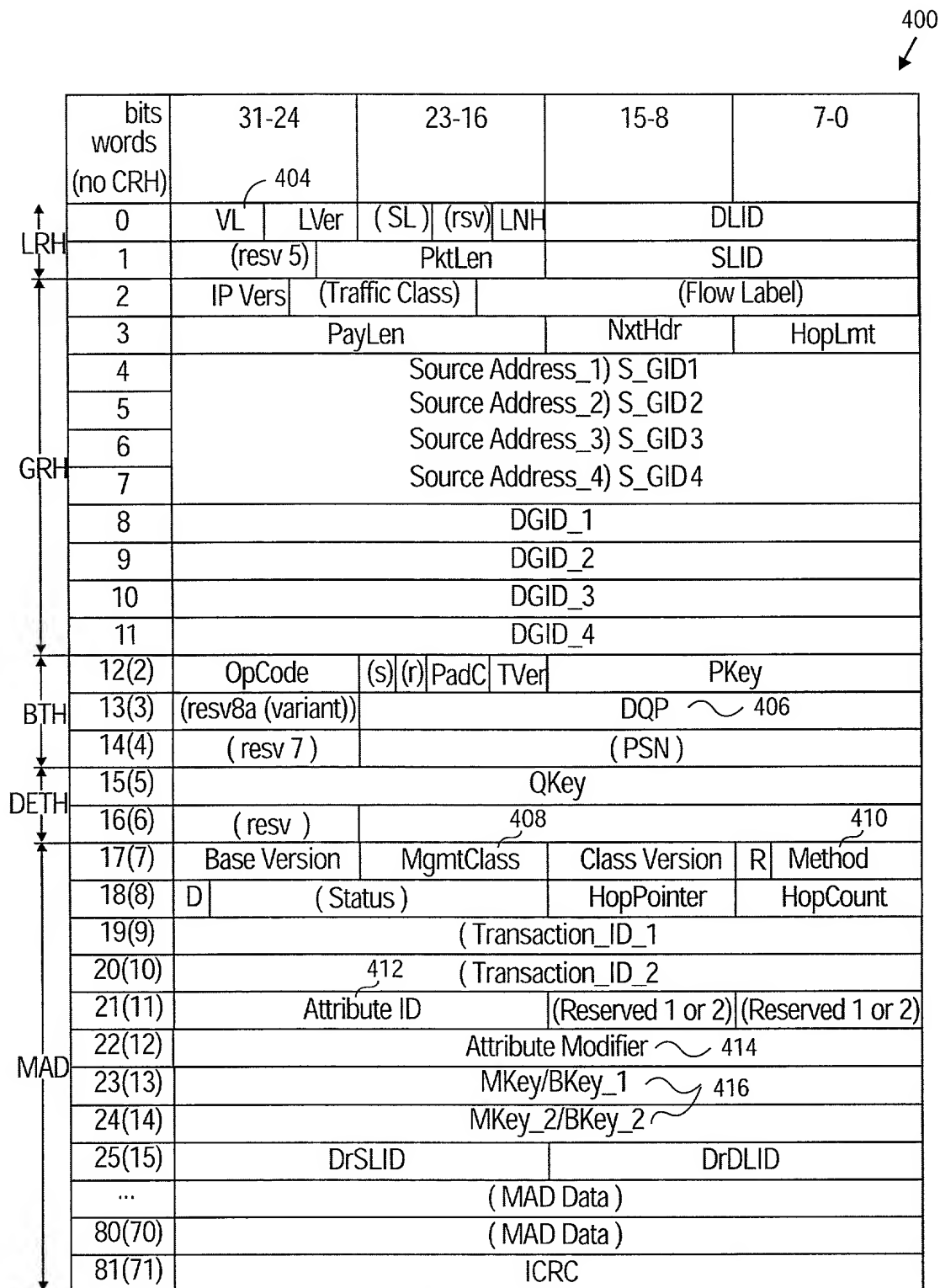


Fig. 4

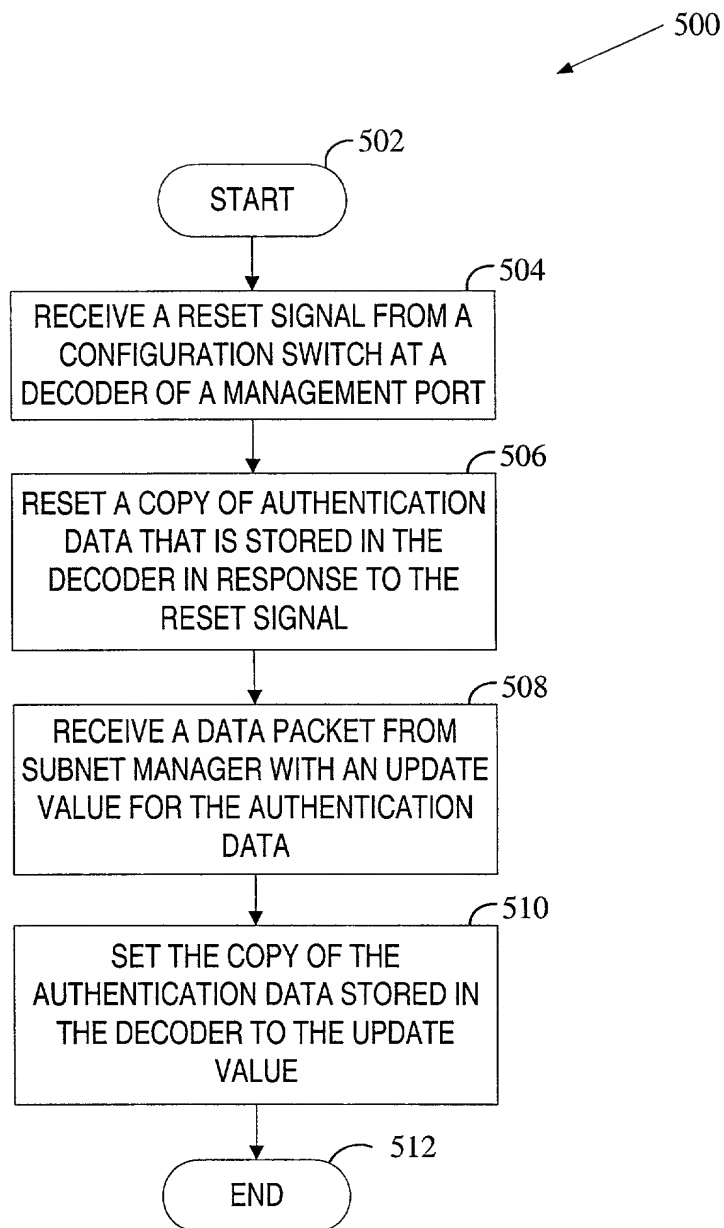


FIG. 5

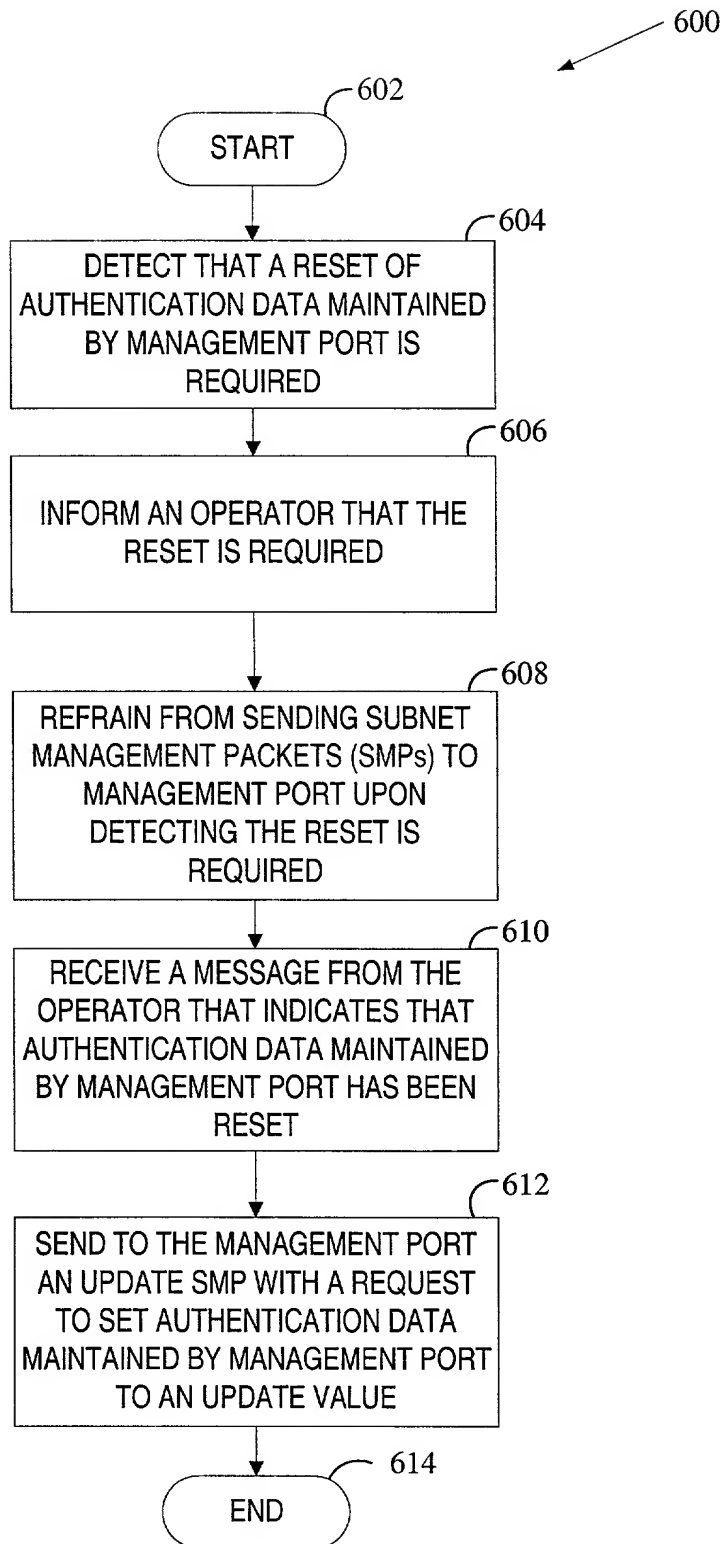


FIG. 6

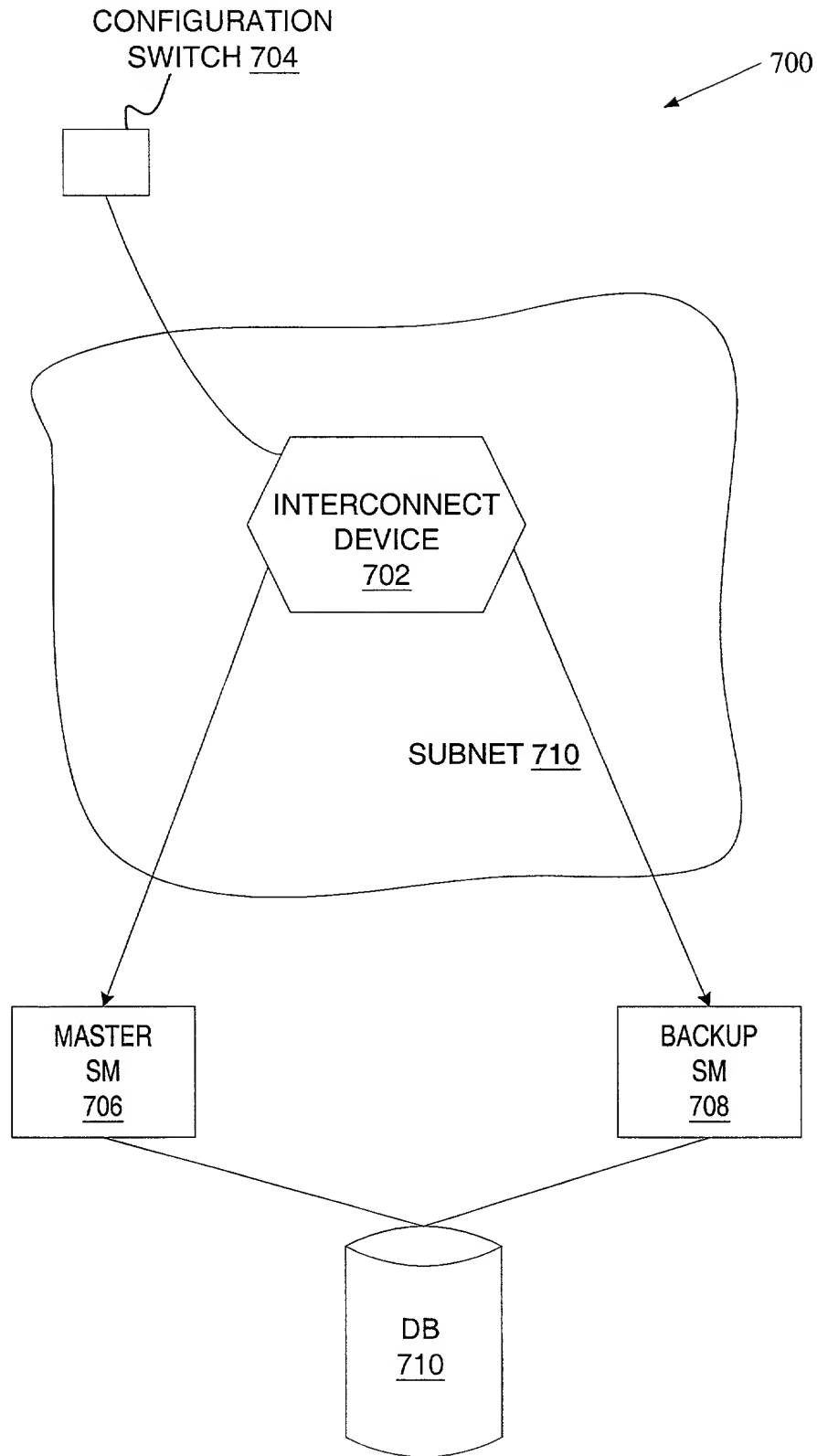


FIG.7A

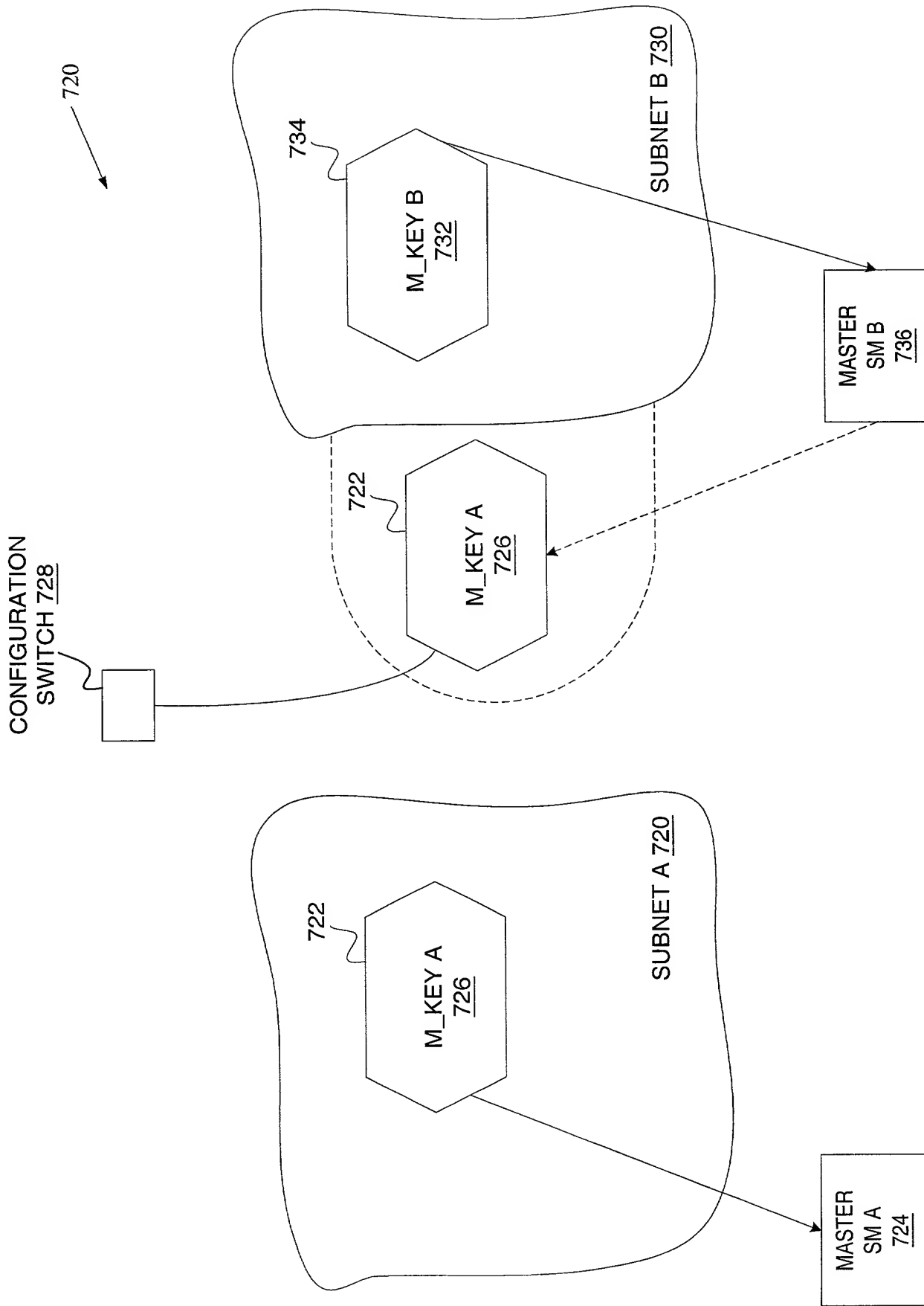


FIG.7B